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概要	In this study, logics and translations for hierarchical model checking are developed based on linear-time temporal logic (LTL), computation-tree logic (CTL), and full computation-tree logic (CTL*). A sequential linear-time temporal logic (sLTL), a sequential computation-tree logic (sCTL), and a sequential full computation-tree logic (sCTL*), which can suitably represent hierarchical information and structures, are developed by extending LTL, CTL, and CTL*, respectively. Translations from sLTL, sCTL, and sCTL* into LTL, CTL, and CTL*, respectively, are defined, and theorems for embedding sLTL, sCTL, and sCTL* into LTL, CTL, and CTL*, respectively, are proved using these translations.